06-12-00

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Attorney's Docket No. 115148

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	
	:	
JOEL WEISSBERGER	:	Group Art Unit: Unknown
MARK McWHIRTER	:	
VALERIU COZLOVSCHI	:	Examiner: Unknown
ERROL GINSBERG	:	
	:	
Serial No.: Not yet assigned	:	
	:	
Filed: Herewith	:	

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor(s):

Joel Weissberger
Mark McWhirter
Valeriu Cozlovschi
Errol Ginsberg

For:

Method of Determining Time Delay for Round Trip Transmission of Data and Electronic Apparatus Therefor

1. Type of Application

This new application is for a(n)

[X] Original (nonprovisional)
[ ] Design
  [ ] Plant
[ ] Divisional
[ ] Continuation
[ ] Continuation-in-part (C-I-P)

Title: Method of Determining Time Delay for Round-Trip Transmission of Data and Electronic Apparatus Therefor

2. Papers Enclosed

A. Required for filing date under 37 CFR § 1.53(b) (Regular) or 37 CFR § 1.153 (Design) Application

14 Pages of specification
14 Pages of claims
6 Sheets of drawing
[ ] The enclosed drawing(s) are photograph(s), and there is also attached a "Petition to Accept Photograph(s) as Drawing(s)." 37 CFR 1.84(b)
[ ] formal
[X] informal

B. Other Papers Enclosed

4 Pages of declaration and power of attorney
2 Pages of abstract

3. Declaration or oath

[X] Enclosed
Executed by
[X] inventor(s).
[ ] legal representative of inventor(s). (37 CFR 1.42 or 1.43)
[ ] joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
[ ] This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 13 below for fee.

[ ] Not enclosed.

4. Inventorship Statement

The inventorship for all the claims in this application are:
[X] The same.
[ ] Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,
[ ] is submitted.
[ ] will be submitted.

5. Language

[X] English
[ ] Non-English
[ ] The attached translation includes a statement that the translation is accurate. 37 CFR 1.52(d).

Title: Method of Determining Time Delay for Round-Trip Transmission of Data and Electronic Apparatus Therefor

6. Assignment

[X] An assignment of the invention to IXIA Communications

[X] is attached. A separate

[ ] "Cover Sheet for Assignment Document Accompanying New Patent Application" or

[X] Form PTO 1595 is also attached.

[ ] will follow.

7. Fee Calculation (37 CFR 1.16)

Regular application

CLAIMS AS FILED					
	Number Filed	Number Extra		Rate	Basic fee 37 CFR 1.16(a) $690.00
Total Claims (37 CFR 1.16(c))	37 - 20 =	17	x	$18.00	$306.00
Independent Claims (37 CFR 1.16(b))	2 - 3 =	0	x	$78.00	$0.00
Multiple dependent Claim(s), if any (37 CFR 1.16(d))	0		x	$260.00	$0.00

Filing Fee Calculation $996.00

9. Small Entity Statement(s)

[X] Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

Filing Fee Calculation (50% of **A, B** or **C** above) $498.00

Title: Method of Determining Time Delay for Round-Trip Transmission of Data and Electronic Apparatus Therefor

10. Fee Payment Being Made at this Time

[ ] Not Enclosed

[ ] No filing fee is to be paid at this time.

[X] Enclosed

[X]	Filing fee	$498.00
[X]	Recording assignment ($40.00; 37 CFR 1.21(h))	$40.00
	Total fees enclosed	$538.00

11. Method of Payment of Fees

[X] Check in the amount of $538.00

12. Authorization to Charge Additional Fees

[X] The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 02-4467:

- [X] 37 CFR 1.16(a), (f) or (g) (filing fees)
- [X] 37 CFR 1.16(b), (c) or (d) (presentation of extra claims)
- [ ] 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- [ ] 37 CFR 1.17(a)(1)-(5) (extension fees pursuant to 1.136(a))
- [ ] 37 CFR 1.17 (application processing fees)
- [ ] 37 CFR 1.18 (issue fee at or before mailing of Notice of Allowance pursuant to 37 CFR 1.311(b))

13. Instructions as to Overpayment

[X] Credit Account No. 02-4467

[ ] Refund

Respectfully submitted,

BRYAN CAVE, LLP

Dated: 09 June 2005

By: _____

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Title: Method of Determining Time Delay for Round-Trip Transmission of Data and Electronic Apparatus Therefor

CERTIFICATE OF EXPRESS MAILING UNDER 37 C.F.R. 1.10.

I hereby certify that this document (and any as referred to as being attached or enclosed) is being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service, mailing label No. **EL312485790US** on June 9, 2000 and addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Cindy Guerrero, Legal Secretary

Inventors: ERROL GINSBERG
VALERIU COZLOVSCHI
JOEL WEISSBERGER
MARK McWHIRTER
Attorney Docket No: 115148

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(Small Business)

I hereby declare that I am an official of, and authorized to act on behalf of, the small entity identified below:

NAME OF ENTITY: IXIA Communications
ADDRESS OF ENTITY: 26601 West Agoura Road
Calabasas, California 91302

I hereby declare that the above identified entity qualifies as a small business concern as defined in 13 C.F.R. § 121.3-18 and reproduced in 37 C.F.R. § 1.9(d), for purposes of paying reduced fees under 35 U.S.C. §§ 41(a) and (b), in that the number of employees of the entity, including those of its affiliates, does not exceed 500 persons. For purposes of this statement: (1) the number of employees of the entity is the average over the previous fiscal year of the entity of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year; and (2) entities are affiliates of each other when either, directly or indirectly, one entity controls or has the power to control the other, or a third party or parties control or have the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the entity identified above with regard to the invention entitled:

METHOD OF DETERMINING TIME DELAY
FOR ROUND-TRIP TRANSMISSION OF DATA
AND ELECTRONIC APPARATUS THEREFOR

filed herewith. If the rights held by the entity identified above are not exclusive, I have identified below each individual, concern, or organization having rights to the invention. (If none write "NONE"). For each such individual, concern, or organization, I have indicated whether such qualifies as an individual, small business concern, or nonprofit organization. I declare that I have not assigned, granted, conveyed, or licensed and am under no obligation under contract or law to assign, grant convey, or license, any rights in the invention to any person or entity that could not be classified as a small entity under 37 C.F.R. § 1.9 (f).

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Inventors: GINSBERG; COZLOVSCHI; WEISSBERGER; and McWHIRTER

Attorney Docket No: 115148

Verified Statement Claiming Small Entity Status

Name	Address	Classification (individual, small business, nonprofit)
NONE		

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 C.F.R. § 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Date: 6/2/00

By: E Ginsberg

Name: Errol Ginsberg

Title: President

Attorney Docket No.: 115148

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Inventors: JOEL WEISSBERGER
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METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Related Application

Related subject matter is disclosed in United States patent application number 09/XXX,XXX filed XXXXX XX, 2000, assigned to the same assignee, having an attorney docket number of 115146, and hereby incorporated by reference.

Field of the Invention

This invention relates, in general, to data transmission, and more particularly, to methods of determine time delay for a round-trip transmission of data and apparatuses therefor.

Background of the Invention

A user accessing a computer server across a computer network must transmit data across the computer network from the user's computer to the computer server and must also receive data across the computer network from the computer server to the user's computer. Therefore, the user requires fast data transmission rates across the computer network and requires, in particular, fast round-trip data transmission across the computer network. However, as computer networks continuously grow in size and complexity, the data transmission rates associated with the larger and more complex computer networks may decrease. Accordingly, a need exists for a method of determining a time delay for the round-trip transmission of data and an apparatus therefor.

Summary of the Invention

In accordance with the principles of the invention, an embodiment of a method of determining a time delay for a round-trip transmission of data comprises receiving a first data packet comprising a first IP source address, a first IP destination address, a first TCP source port, a first TCP destination port, and a first time stamp indicating a first time when the first data packet was transmitted. The method continues by inserting the first IP destination address as a second IP source address in a second data packet and by inserting the first IP source address as a second IP destination address in the second data packet. Next, the method proceeds by inserting the first TCP destination port as a second TCP source port in the second data packet and by inserting the first TCP source port as a second TCP destination port in the second data packet. Then, the method continues by inserting the first time stamp as a second time stamp in the second data packet and by transmitting the second data packet.

Further, in accordance with the principles of the invention, an embodiment of an electronic apparatus for determining a time delay for a round-trip transmission of data comprises a data reception portion, an input memory portion coupled to the data reception portion, a data validity portion coupled to the data reception portion, and a first memory and data transfer management portion coupled to the input memory portion and the data validity portion. The electronic apparatus further comprises a second memory and data transfer management portion coupled to the first memory and data transfer management portion, an output memory portion coupled to the input memory portion and the second memory and data transfer management portion, and a data pattern management portion coupled to the second memory and data transfer management portion. The electronic apparatus additionally comprises a header format portion

coupled to the output memory portion and a data transmission portion coupled to the header format portion and the data pattern management portion.

Brief Description of the Drawing

The invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which:

FIG. 1 illustrates a block diagram of an electronic apparatus for determining a time delay of a round-trip transmission of data in accordance with an embodiment of the invention;

FIG. 2 illustrates a flow chart for a method of determining a time delay for a round-trip transmission of data in accordance with an embodiment of the invention; and

FIGs. 3 through 6 illustrate flow charts of detailed portions of the method of FIG. 2 in accordance with an embodiment of the invention.

For simplicity and clarity of illustration, the same reference numerals in different figures denote the same elements, and descriptions and details of well-known features and techniques are omitted to avoid unnecessarily obscuring the invention.

Furthermore, the terms first, second, third, fourth, and the like in the description and in the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. However, it is understood that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein. It is further understood that the terms so used are interchangeable under appropriate circumstances.

Detailed Description

FIG. 1 illustrates a block diagram of an electronic device or apparatus 100 for determining a time delay of a round-trip transmission of data. Electronic apparatus 100 comprises an incoming data portion and an outgoing data portion. The incoming data portion includes a data reception portion 110, an input memory portion 115, a data validity portion 120, and, a first memory and data transfer management portion 125. Input memory portion 115 and data validity portion 120 are both coupled to data reception portion 110. Memory and data transfer management portion 125 is coupled to both of input memory portion 115 and data validity portion 120.

The outgoing data portion of electronic apparatus 100 comprises a second memory and data transfer management portion 150, an output memory portion 155, a data pattern management portion 160, a header format portion 165, and a data transmission portion 170. Memory and data transfer management portion 150 is coupled to memory and data transfer management portion 125. Output memory portion 155 is coupled to both of input memory portion 115 and memory and data transfer management portion 150. Data pattern management portion 160 is coupled to memory and data transfer management portion 150 and data transmission portion 170. Header format portion 165 is coupled to output memory portion 155, and data transmission portion 170 is coupled to header format portion 165.

In the preferred embodiment, the incoming and outgoing data portions of electronic apparatus 100 are formed within a single field-programmable gate array (FPGA), as indicated by a dashed line 105. For example, memory portions 115, 155, memory and data transfer management portions 125, 150, data validity portion 120, data reception portion 110, data

transmission portion 170, header format portion 165, and data pattern management portion 160 can be located within the single FPGA.

Electronic apparatus 100 further comprises a data pattern memory portion 190 coupling data pattern management portion 160 to data transmission portion 170. In the preferred embodiment, data pattern memory portion 190 is not included in the FPGA. Instead, data pattern memory portion 190 is a preferably a separate dynamic random access memory (DRAM).

As a brief overview of the operation of electronic apparatus 100, data reception portion 110 receives an incoming data packet or frame, and data validity portion 120 validates the incoming data packet. Input memory portion 115 receives a portion of the incoming data packet from data reception portion 110, and input memory portion 115 stores the portion of the incoming data packet. The portion of the incoming data packet comprises, among other items, an Internet Protocol (IP) source address, an IP destination address, a Transport Control Protocol (TCP) source port, a TCP destination port, and a time stamp. Memory and data transfer management portions 125, 150 interact or cooperate to manage a transfer of the stored portions of the incoming data packet from input memory portion 115 to output memory portion 155. Output memory portion 155 receives the portion of the incoming data packet from input memory portion 115, and output memory portion 155 stores the portion of the incoming data packet. Header format portion 165 takes the portion of the incoming data packet and inserts it into an outgoing data packet transmitted out of electronic apparatus 100 through data transmission portion 170. Data pattern management portion 160 manages an insertion of a data pattern from data pattern memory portion 190 into the outgoing data packet from data transmission portion 170. The operation of electronic apparatus 100 is described in more detail with reference to FIGs. 2 through 6.

FIG. 2 illustrates a flowchart for a method 200 of determining a time delay for a round-trip transmission data. A first electronic device or apparatus transmits a first data packet at a first time where the first electronic apparatus has a first IP source address and a first TCP source port. In the preferred embodiment, the first data packet comprises the first IP source address, a first IP destination address, a first IP checksum, the first TCP source port, a first TCP destination port, a first set of six TCP flags, a first TCP checksum, a first data pattern, a first time stamp indicating the first time when the first data packet was transmitted from the first electronic apparatus, and a first Checklist Redundancy Check (CRC) checksum. A second electronic device or apparatus, such as electronic apparatus 100 of FIG. 1 waits for the first data packet. The second electronic apparatus has the first IP destination address and the first TCP destination port.

At a step 205 of method 200 in FIG. 2, the second electronic apparatus begins to receive the first data packet transmitted from the first electronic apparatus. Upon beginning to receive the first data packet, the second electronic apparatus checks a status of a first memory portion within the second electronic apparatus. As an example, referring back to FIG. 1, as data reception portion 110 begins to receive the first data packet, memory and data transfer management portion 125 checks the status of input memory portion 115. If the status of input memory portion 115 is full, then method 200 (FIG. 2) terminates or starts over by waiting for a new data packet and begins receiving the new data packet at step 205 (FIG. 2). However, if the status of input memory portion 115 is empty or if input memory portion 115 has enough empty memory to store desired portions of the first data packet, then data reception portion 110 begins identifying different portions of the first data packet while receiving the first data packet. In the preferred embodiment, input memory portion 115 is large enough to store the desired portions of two data packets. Electronic apparatus 100 stores the identified portions of the first data packet

within input memory portion 115 while receiving the first data packet. Data validity portion 120 validates the different portions of the first data packet while electronic apparatus 100 receives the different portions of the first data packet.

Returning to FIG. 2, step 205 of method 200 also begins the calculation of a CRC checksum for the first data packet. This calculation begins with the first byte of data of the first data packet and preferably starts upon receiving the first byte of data of the first data packet. Next, steps 210, 215, and 220 of method 200 briefly describe the identifying, storing, and validating steps described in the previous paragraph. At step 210, the second electronic apparatus identifies, stores, and validates portions of an IP header of the first data packet, and at a step 215, the second electronic apparatus identifies, stores, and validates portions of a TCP header of the first data packet. At step 220, the second electronic apparatus identifies and stores the time stamp of the first data packet. Steps 210 and 215 are described in more detailed hereinafter with respect to FIGs. 3 and 4, respectively.

At a step 225 of method 200, the second electronic apparatus stops receiving the first data packet. Then, at a step 230, the second electronic apparatus validates the entire first data packet based on a CRC checksum match. As an example, the second electronic apparatus can perform step 230 by comparing the calculated and received CRC checksums. If the calculated and received CRC checksums are not equal to each other, then method 200 terminates or starts over by waiting for a new data packet and begins receiving the new data packet at step 205. However, if the calculated and received CRC checksums are equal to each other, then method 200 continues such that the second electronic apparatus sets or changes the status of the first memory portion storing the portions of the first data packet from empty to full.

Then, the second electronic apparatus checks a status of a second memory portion within the second electronic apparatus. If the status of the second memory portion is full, then the second electronic apparatus waits until at least a portion of the second memory potion is free, is empty, or otherwise becomes available. This portion of the second memory portion needs to be large enough to store the portions of the first data packet currently stored in the first memory portion. After the portion of the second memory becomes available, the second electronic apparatus transfers the stored portions of the first data packet from the first memory portion to the second memory portion. Then, the second electronic apparatus sets or changes the status of the second memory portion from empty to full, and the second electronic apparatus also sets or changes the status of the first memory portion from full to empty. As an example, referring back to FIG. 1, memory and data transfer management portions 125, 150 cooperate or interact to transfer the stored portions of the first data packet from input memory portion 115 to output memory portion 155. In the preferred embodiment, steps 210, 215, and 220 in FIG. 2 are performed in real-time while simultaneously receiving the first data packet.

Returning to FIG. 2, method 200 continues at a step 235 where the second electronic apparatus begins transmitting a second data packet back to the first electronic apparatus. Step 235 of method 200 also begins the calculation of a CRC checksum for the second data packet. This calculation begins with the first byte of data of the second data packet. At a step 240, the second electronic apparatus inserts the stored portions of the IP header of the first data packet into an IP header of the second data packet, and at a step 245, the second electronic apparatus inserts the stored portions of the TCP header of the first data packet into a TCP header of the second data packet. As an example, header format portion 165 (FIG. 1), output memory portion 155 (FIG. 1), and data transmission portion 170 (FIG. 1) can perform steps 240 and 245 in FIG.

2. Steps 240 and 245 are described in more detailed hereinafter with respect to FIGs. 5 and 6, respectively.

Returning back to FIG. 2, at a step 250 of method 200, the second electronic apparatus sends or transmits a second data pattern as part of the second data packet. The second data pattern of the second data packet can be the same as or different from the first data pattern in the first data packet. As an example, data pattern management portion 160 (FIG. 1), data pattern memory portion 190 (FIG. 1), and data transmission portion 170 (FIG. 1) can perform step 250.

Subsequently, at a step 255 of method 200, the second electronic apparatus inserts the first time stamp of the first data packet stored in the second memory portion as a second time stamp in the second data packet. Next, at a step 260, the second electronic apparatus inserts a validity check for the second data packet into the second data packet. As an example, the validity check is a second CRC checksum that is different from the first CRC checksum of the first data packet. In the preferred embodiment, header format portion 165 (FIG. 1), output memory portion 155 (FIG. 1), and data transmission portion 170 (FIG. 1) perform steps 255 and 260. Subsequently, at a step 265 of method 200, the second electronic apparatus stops transmitting the second data packet. In the preferred embodiment, steps 240, 245, 250, 255, and 260 are performed in real-time while simultaneously transmitting the second data packet.

Next, the first electronic apparatus receives the second data packet at a second time. This second time occurs after the first time at which the first electronic apparatus originally transmitted the first data packet to the second electronic apparatus. The first electronic apparatus determines the time delay for the round-trip transmission of data from the first electronic apparatus to the second electronic apparatus and back to the first electronic apparatus by subtracting the time indicated by the second time stamp in the second data packet from the

second time. As indicated earlier at step 255, the second time stamp in the second data packet contains the first time at which the first electronic apparatus transmitted the first data packet.

FIG. 3 illustrates a flowchart of substeps within step 210 of FIG. 2. At a step 310 in FIG. 3, the second electronic apparatus identifies a beginning of the IP header in the first data packet, and at a step 320, the second electronic apparatus begins calculating an IP checksum for the first data packet. At a step 330, the second electronic apparatus identifies an IP source address within the IP header of the first data packet, and at a step 340, the second electronic apparatus stores the first IP source address. Then, at a step 350, the second electronic apparatus identifies an IP destination address in the IP header of the first data packet, and at a step 360, the second electronic apparatus stores the IP destination address. Next, at a step 370, the second electronic apparatus identifies an end of the IP header, and, at a step 380, the second electronic apparatus validates the IP header data of the first data packet based on an IP checksum match.

To perform step 380, the second electronic apparatus finishes calculating the IP checksum for the first data packet and compares the calculated IP checksum to the received IP checksum of the first data packet. If the calculated and received IP checksums are equal to each other, then the IP checksum of the first data packet is valid, and method 200 (FIG. 2) continues with step 215 (FIG. 2). However, if the calculated and received IP checksums are not equal to each other, then method 200 (FIG. 2) terminates or starts over, and the second electronic apparatus waits for another data packet and begins receiving the other data packet at step 205 (FIG. 2). In the preferred embodiment, steps 310, 320, 330, 340, 350, 360, 370, and 380 are performed in real-time while simultaneously receiving the first data packet. Also in the preferred embodiment, the second electronic apparatus identifies and stores the IP source and destination addresses before validating the IP header data.

FIG. 4 illustrates a flowchart of the substeps within step 215 of FIG. 2. At a step 410 of FIG. 4, the second electronic apparatus identifies a beginning of the TCP header in the first data packet. Then, at a step 415, the second electronic apparatus begins to calculate a TCP checksum for the first data packet. Next, at a step 420, the second electronic apparatus identifies a TCP source port in the TCP header of the first data packet, and a step 430, the second electronic apparatus stores the TCP source port. At a step 440, the second electronic apparatus identifies a TCP destination port in the TCP header of the first data packet, and at a step 450, the second electronic apparatus stores the TCP destination port. Then, at a step 460, the second electronic apparatus identifies the TCP flags in the TCP header of the first data packet, and at a step 470, the second electronic apparatus stores at least a portion of the TCP flags. In the preferred embodiment, the second electronic apparatus receives six TCP flags in the first data packet, but stores only two of the six TCP flags. In particular, the second electronic apparatus stores the TCP flags identified as a final (FIN) flag and a synchronous (SYN) flag. Next, at a step 480, the second electronic apparatus identifies an end of the TCP data, and at a step 490, the second electronic apparatus validates the TCP data, including the TCP header, in the first data packet based on a TCP checksum match.

As an example, the second electronic apparatus can perform step 490 by comparing the calculated and received TCP checksums. If the calculated and received TCP checksums are equal to each other, then method 200 (FIG. 2) continues with step 220 (FIG. 2). However, if the calculated and received checksums are not equal to each other, then method 200 (FIG. 2) terminates or starts over, and the second electronic apparatus waits to receive another data packet and begins receiving the new data packet at step 205 (FIG. 2). Also in the preferred embodiment, the second electronic apparatus performs steps 410, 420, 430, 440, 450, 460, 470,

480, and 490 in real-time while simultaneously receiving the first data packet. Furthermore, the second electronic apparatus preferably identifies and stores the TCP source and destination ports and the TCP flags before validating the TCP data.

FIG. 5 illustrates a flowchart of the substeps in step 240 of FIG. 2. At a step 510 of FIG. 6, the second electronic apparatus counts an IP header offset, and at a step 520, the second electronic apparatus calculates a second IP checksum for the second data packet. Step 520 can be performed at this time because the portions of the IP header used to calculate IP checksum are already known and stored in the second memory portion. Next, at a step 530, the second electronic apparatus adds an IP checksum offset to the IP header offset, and at a step 540, the second electronic apparatus inserts the calculated IP checksum into the second data packet. Next, at a step 550, the second electronic apparatus adds an IP source address offset to the previous offset sum, and then the second electronic apparatus uses the first IP destination address of the first data packet stored in the second memory portion. In particular, at a step 560, the second electronic apparatus inserts the first IP destination address as a second IP source address in the second data packet.

Then, at a step 570, the second electronic apparatus adds an IP destination address offset to the previous offset sum, and then the second electronic apparatus uses the first IP source address of the first data packet stored in the second memory portion. In particular, at a step 580, the second electronic apparatus inserts the first IP source address as a second IP destination address in the second data packet. In the preferred embodiment, the second electronic apparatus performs steps 520, 530, and 540 before steps 550, 560, 570, and 580. Also in the preferred embodiment, the second electronic apparatus performs steps 510, 520, 530, 540, 550, 560, 570, and 580 in real-time while simultaneously transmitting the second data packet.

FIG. 6 illustrates a flowchart of the substeps of step 245 in FIG. 2. At a step 610 in FIG. 6, the second electronic apparatus counts a TCP header offset, and at a step 620, the second electronic apparatus adds a TCP source port offset to the TCP header offset. Then, the second electronic apparatus uses the first TCP destination port of the first data packet stored in the second memory portion. In particular, at a step 630, the second electronic apparatus inserts the first TCP destination port as a second TCP source port in the second data packet. Next, at a step 640, the second electronic apparatus adds a TCP destination port offset to the previous offset sum, and then the second electronic apparatus uses the first TCP source port of the first data packet stored in the second memory portion. In particular, at a step 650, the second electronic apparatus inserts the first TCP source port as a second TCP destination port in the second data packet.

Subsequently, at a step 660, the second electronic apparatus adds a TCP flag offset to the previous offset sum, and then the second electronic apparatus uses the two TCP flags of the first data packet stored in the second memory portion. In particular, at a step 670, the second electronic apparatus inserts the FIN flag and the SYN flag as a portion of the second TCP flags into the second data packet. The second electronic apparatus also inserts four other TCP flags, for a total of six TCP flags, into the second data packet. In particular, the second electronic apparatus inserts a TCP flag identified as an acknowledgment (ACK) flag where the ACK flag has a value of one. The second electronic apparatus also inserts three other TCP flags, each having a value of zero.

Then, at a step 680, the second electronic apparatus adds a TCP checksum offset to the previous offset sum, and at a step 690, the second electronic apparatus calculates and inserts the second TCP checksum into the second data packet. In the preferred embodiment, the second

electronic apparatus component begins and finishes calculating the second TCP checksum after step 680. Also in the preferred embodiment, the second electronic apparatus performs steps 610, 620, 630, 640, 650, 660, and 670 before steps 680 and 690. Furthermore, the second electronic apparatus preferably performs steps 610, 620, 630, 640, 650, 660, 670, 680, and 690 in real-time while simultaneously transmitting the second data packet.

Therefore, an improved method of determining a time delay for the round-trip transmission of data and an apparatus therefor are provided to overcome the disadvantages of the prior art. The method and apparatus enable the detection of an increase or decrease in the time delay for the round-trip transmission of data across a computer network.

Although the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made without departing from the spirit or scope of the invention. For instance, the numerous details set forth herein such as, for example, the specific sequence of steps are provided to facilitate the understanding of the invention and are not provided to limit the scope of the invention. Furthermore, the method described herein is not limited to the round-trip transmission of data between two electronic devices. Instead, the method can be modified and applied to the round-trip or non-round-trip transmission of data between three or more electronic devices. Accordingly, the disclosure of embodiments of the invention is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the scope of the invention shall be limited only to the extent required by the appended claims.

CLAIMS

1. A method of determining a time delay for a round-trip transmission of data comprising:

receiving a first data packet comprising a first IP source address, a first IP destination address, a first TCP source port, a first TCP destination port, and a first time stamp indicating a first time when the first data packet was transmitted;

inserting the first IP destination address as a second IP source address in a second data packet;

inserting the first IP source address as a second IP destination address in the second data packet;

inserting the first TCP destination port as a second TCP source port in the second data packet;

inserting the first TCP source port as a second TCP destination port in the second data packet;

inserting the first time stamp as a second time stamp in the second data packet; and

transmitting the second data packet.

2. The method of claim 1 further comprising:

transmitting the first data packet at the first time;

receiving the second data packet at a second time; and

determining a difference between the first time in the second time stamp and the second time to establish the time delay for the round-trip transmission of data.

3. The method of claim 1 further comprising:

validating the first IP destination address while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, and before transmitting the second data packet; and

validating the first TCP destination port while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, and before transmitting the second data packet.

4. The method of claim 1 wherein:

inserting the first IP destination address occurs while transmitting the second data packet; and

inserting the first IP source address occurs while transmitting the second data packet.

5. The method of claim 1 wherein:

inserting the first TCP destination port occurs while transmitting the second data packet; and

inserting the first TCP source port occurs while transmitting the second data packet.

6. The method of claim 1 wherein:

inserting the first time stamp occurs while transmitting the second data packet.

7. The method of claim 1 further comprising:

providing the first data packet to further comprise a first IP checksum, a first TCP checksum, and a first CRC checksum;

validating the first IP checksum while receiving the first data packet;

validating the first TCP checksum while receiving the first data packet; and

validating the first CRC checksum.

8. The method of claim 7 further comprising:

storing the first IP source address and the first IP destination address before validating the first IP checksum; and

storing the first TCP source port and the first TCP destination port after validating the first IP checksum and before validating the first TCP checksum.

9. The method of claim 7 wherein:

validating the first TCP checksum occurs after validating the first IP checksum and before validating the first CRC checksum.

10. The method of claim 7 wherein:

validating the first CRC checksum occurs after receiving the first data packet.

11. The method of claim 7 further comprising:

determining a second IP checksum for the second data packet;

inserting the second IP checksum into the second data packet while transmitting the second data packet;

determining a second TCP checksum for the second data packet; and

inserting the second TCP checksum into the second data packet while transmitting the second data packet.

12. The method of claim 11 wherein:

inserting the first IP destination address occurs while transmitting the second data packet;

inserting the first IP source address occurs while transmitting the second data packet;

inserting the first TCP destination port occurs while transmitting the second data packet;

inserting the first TCP source port occurs while transmitting the second data packet; and

inserting the first time stamp occurs while transmitting the second data packet.

13. The method of claim 11 wherein:

inserting the first IP destination address occurs after inserting the second IP checksum;

inserting the first IP source address occurs after inserting the first IP destination address;

inserting the first TCP destination port occurs after inserting the first IP source address; and

inserting the first TCP source port occurs after inserting the first TCP destination port and before inserting the second TCP checksum.

14. The method of claim 1 further comprising:

providing the first data packet to further comprise a first data pattern; and

inserting a second data pattern into the second data packet.

15. The method of claim 14 wherein:

inserting the second data pattern occurs while transmitting the second data packet.

16. The method of claim 1 further comprising:

providing the first data packet to further comprise a first TCP flag; and

inserting the first TCP flag as a second TCP flag into the second data packet.

17. The method of claim 16 further comprising:

validating the first TCP flag while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, before transmitting the second data packet, and before inserting the first TCP flag.

18. The method of claim 16 wherein:

inserting the second TCP flag occurs while transmitting the second data packet.

19. The method of claim 1 further comprising:

providing the first data packet to further comprise two TCP flags;

inserting the two TCP flags into the second data packet;

inserting an additional TCP flag into the second data packet, the additional TCP flag having a value of one; and

inserting three additional TCP flags into the second data packet, the three additional TCP flags each having a value of zero.

20. The method of claim 1 further comprising:

providing the first data packet to further comprising six TCP flags;

inserting two of the six TCP flags into the second data packet;

inserting an additional TCP flag into the second data packet, the additional TCP flag having a value of one; and

inserting three additional TCP flags into the second data packet, the three additional TCP flags each having a value of zero.

21. The method of claim 20 further comprising:

providing a FIN flag and a SYN flag for the two of the six TCP flags; and

providing an ACK flag for the additional TCP flag.

22. The method of claim 1 further comprising:

providing the first data packet to further comprise a first IP checksum, first TCP flags, a first TCP checksum, and a first CRC checksum;

validating the first IP checksum while receiving the first data packet;

validating the first TCP checksum while receiving the first data packet;

validating the first CRC checksum after receiving the first data packet;

determining a second IP checksum for the second data packet;

inserting and the second IP checksum into the second data packet while transmitting the second data packet;

inserting the first TCP flags as second TCP flags into the second data packet while transmitting the second data packet;

determining a second TCP checksum for the second data packet;

inserting the second TCP checksum into the second data packet while transmitting the second data packet;

determining a second CRC checksum for the second data packet; and

inserting the second CRC checksum into the second data packet while transmitting the second data packet.

23. The method of claim 22 wherein:

inserting the first IP destination address occurs while transmitting the second data packet;

inserting the first IP source address occurs while transmitting the second data packet;

inserting the first TCP destination port occurs while transmitting the second data packet;

inserting the first TCP source port occurs while transmitting the second data packet; and

inserting the first time stamp occurs while transmitting the second data packet.

24. The method of claim 23 wherein:

inserting the first IP destination address occurs after inserting the second IP checksum;

inserting the first IP source address occurs after inserting the first IP destination address;

inserting the first TCP destination port occurs after inserting the first IP source address;

inserting the first TCP source port occurs after inserting the first TCP destination port;

inserting the first TCP flags occurs after inserting the first TCP source port;

inserting the second TCP checksum occurs after inserting the first TCP flags;

inserting the first time stamp occur after inserting the second TCP checksum; and

inserting the second CRC checksum occurs after inserting the first time stamp.

25. The method of claim 24 further comprising:

providing the first data packet to further comprise a first data pattern; and

inserting a second data pattern into the second data packet while transmitting the second data packet.

26. The method of claim 25 further comprising:

transmitting the first data packet at the first time from a first electronic apparatus having the first IP source address and the first TCP source port;

receiving the second data packet at a second time and at the first electronic apparatus having the second IP destination address and the second TCP destination port; and

subtracting the first time in the second time stamp from the second time to determine the time delay for the round-trip transmission of data,

wherein:

receiving the first data packet further comprises receiving the first data packet at a second electronic apparatus having the first IP destination address and the first TCP destination port; and

transmitting the second data packet further comprises transmitting the second data packet from the second electronic apparatus having the second IP source address and the second TCP source port.

27. The method of claim 22 wherein:

inserting the first IP destination address occurs after inserting the second IP checksum;

inserting the first IP source address occurs after inserting the first IP destination address;

inserting the first TCP destination port occurs after inserting the first IP source address;

inserting the first TCP source port occurs after inserting the first TCP destination port;

inserting the first TCP flags occurs after inserting the first TCP source port;

inserting the second TCP checksum occurs after inserting the first TCP flags;

inserting the first time stamp occur after inserting the second TCP checksum; and

inserting the second CRC checksum occurs after inserting the first time stamp.

28. The method of claim 22 further comprising:

providing the first data packet to further comprise a first data pattern; and

inserting a second data pattern into the second data packet while transmitting the second data packet.

29. The method of claim 22 further comprising:

transmitting the first data packet at the first time from a first electronic apparatus having the first IP source address and the first TCP source port;

receiving the second data packet at a second time and at the first electronic apparatus having the second IP destination address and the second TCP destination port; and

subtracting the first time in the second time stamp from the second time to determine the time delay for the round-trip transmission of data,

wherein:

receiving the first data packet further comprises receiving the first data packet at a second electronic apparatus having the first IP destination address and the first TCP destination port; and

transmitting the second data packet further comprises transmitting the second data packet from the second electronic apparatus having the second IP source address and the second TCP source port.

30. The method of claim 1 further comprising:

waiting for the first data packet;

checking a status of a first memory portion;

storing a portion of the first data packet if the first memory portion is available, the portion of the first memory portion comprising the first IP source address, the first IP destination address, the first TCP source port, and the first TCP destination port;

checking a validity of the first data packet;

setting the status of the first memory portion to full if the first data packet is valid;

checking a status of a second memory portion;

transferring the portion of the first data packet from the first memory portion to the second memory portion if the second memory portion is available and if the first data packet is valid;

setting the status of the second memory portion to full; and

setting the status of the first memory portion to empty.

31. An electronic apparatus for determining a time delay for a round-trip transmission of data comprising:

a data reception portion;

an input memory portion coupled to the data reception portion;

a data validity portion coupled to the data reception portion;

a first memory and data transfer management portion coupled to the input memory portion and the data validity portion;

a second memory and data transfer management portion coupled to the first memory and data transfer management portion;

an output memory portion coupled to the input memory portion and the second memory and data transfer management portion;

a data pattern management portion coupled to the second memory and data transfer management portion;

a header format portion coupled to the output memory portion; and

a data transmission portion coupled to the header format portion and the data pattern management portion.

32. The electronic apparatus of claim 31 further comprising:

an incoming data portion comprising:

the data reception portion;

the input memory portion;

the data validity portion; and

the first memory and data transfer management portion; and

an outgoing data portion comprising:

the second memory and data transfer management portion;

the output memory portion;

the data pattern management portion;

the header format portion; and

the data transmission portion.

33. The electronic apparatus of claim 31 wherein:

the input memory portion stores a portion of an incoming data packet;

the first and second memory and data transfer management portions manage a transfer of the portion of the incoming data packet from the input memory portion to the output memory portion;

the data validity portion validates the incoming data packet;

the output memory portion receives the portion of the incoming data packet from the input memory portion;

the data pattern management portion manages an insertion of a data pattern into an outgoing data packet; and

a header format portion inserts an IP source address, an IP destination address, a TCP source port, a TCP destination port, TCP flags, and a time stamp into the outgoing data packet.

34. The electronic apparatus of claim 31 wherein:

the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array.

35. The electronic apparatus of claim 31 further comprising:

a data pattern memory portion coupling the data pattern management portion to the data transmission portion.

36. The electronic apparatus of claim 35 wherein:

the data pattern memory portion is a dynamic random access memory.

37. The electronic apparatus of claim 36 wherein:

the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array.

METHOD OF DETERMINING TIME DELAY
FOR ROUND-TRIP TRANSMISSION OF DATA AND
ELECTRONIC APPARATUS THEREFOR

Abstract of the Disclosure

A method of determining a time delay for a round-trip transmission of data includes receiving a first data packet having a first IP source address, a first IP destination address, a first TCP source port, a first TCP destination port, and a first time stamp indicating a first time when the first data packet was transmitted. The method continues by inserting the first IP destination address as a second IP source address in a second data packet and by inserting the first IP source address as a second IP destination address in the second data packet. Next, the method proceeds by inserting the first TCP destination port as a second TCP source port in the second data packet and by inserting the first TCP source port as a second TCP destination port in the second data packet. Then, the method continues by inserting the first time stamp as a second time stamp in the second data packet and by transmitting the second data packet.

An electronic apparatus for determining a time delay for a round-trip transmission of data includes a data reception portion, an input memory portion coupled to the data reception portion, a data validity portion coupled to the data reception portion, and a first memory and data transfer management portion coupled to the input memory portion and the data validity portion. The electronic apparatus further includes a second memory and data transfer management portion coupled to the first memory and data transfer management portion, an output memory portion coupled to the input memory portion and the second memory and data transfer management portion, and a data pattern management portion coupled to the second memory and data transfer

management portion. The electronic apparatus additionally includes a header format portion coupled to the output memory portion and a data transmission portion coupled to the header format portion and the data pattern management portion.

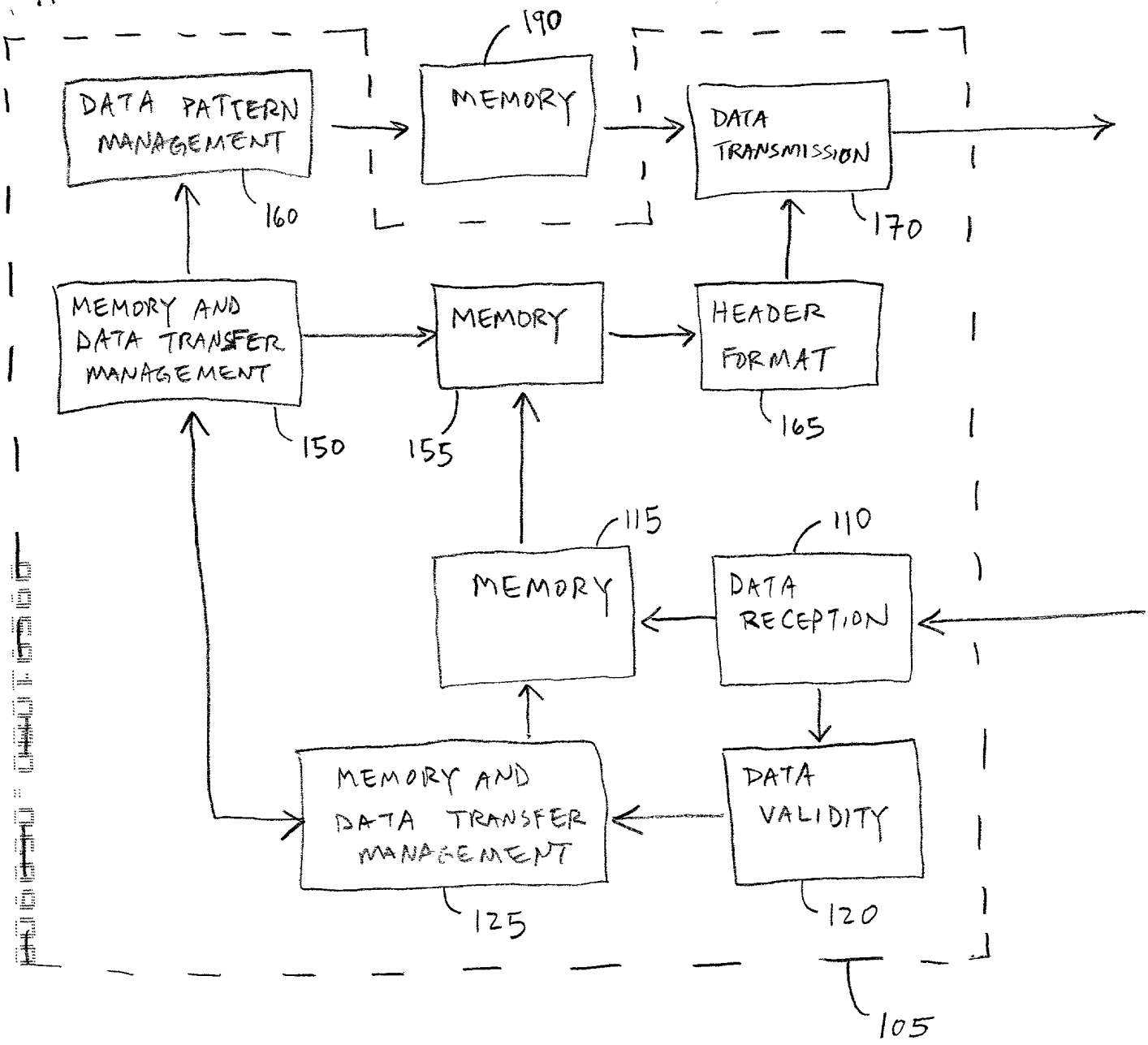

190
MEMORY
DATA PATTERN MANAGEMENT
160
DATA TRANSMISSION
170
MEMORY AND DATA TRANSFER MANAGEMENT
150
MEMORY
155
HEADER FORMAT
165
115
MEMORY
110
DATA RECEPTION
MEMORY AND DATA TRANSFER MANAGEMENT
125
DATA VALIDITY
120
105

FIG. 1

100

FIG. 2

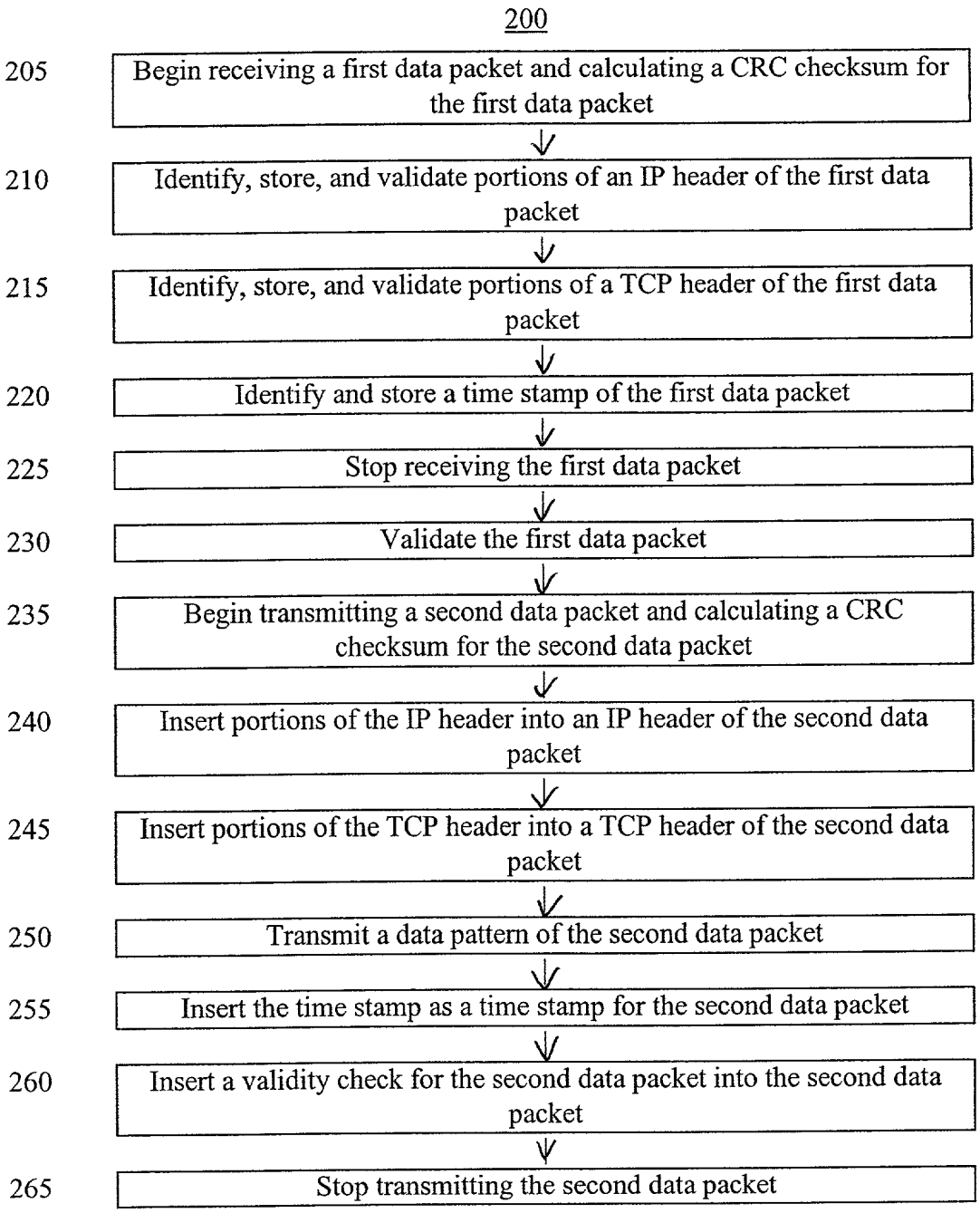

200
205
Begin receiving a first data packet and calculating a CRC checksum for the first data packet
210
Identify, store, and validate portions of an IP header of the first data packet
215
Identify, store, and validate portions of a TCP header of the first data packet
220
Identify and store a time stamp of the first data packet
225
Stop receiving the first data packet
230
Validate the first data packet
235
Begin transmitting a second data packet and calculating a CRC checksum for the second data packet
240
Insert portions of the IP header into an IP header of the second data packet
245
Insert portions of the TCP header into a TCP header of the second data packet
250
Transmit a data pattern of the second data packet
255
Insert the time stamp as a time stamp for the second data packet
260
Insert a validity check for the second data packet into the second data packet
265
Stop transmitting the second data packet

FIG. 3

210

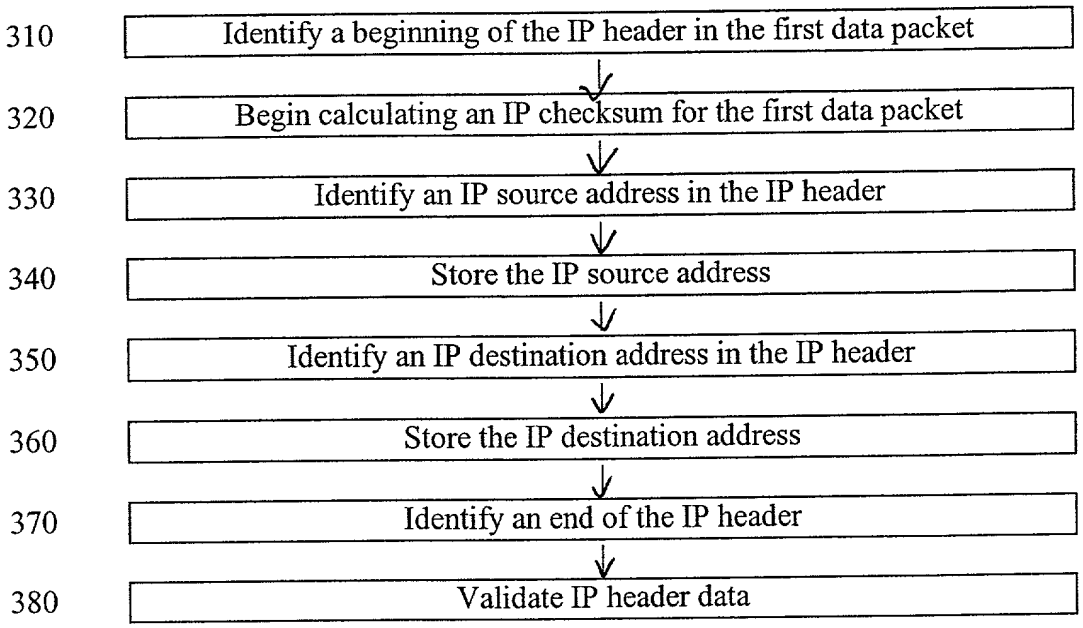

310
Identify a beginning of the IP header in the first data packet
320
Begin calculating an IP checksum for the first data packet
330
Identify an IP source address in the IP header
340
Store the IP source address
350
Identify an IP destination address in the IP header
360
Store the IP destination address
370
Identify an end of the IP header
380
Validate IP header data

FIG. 4

215

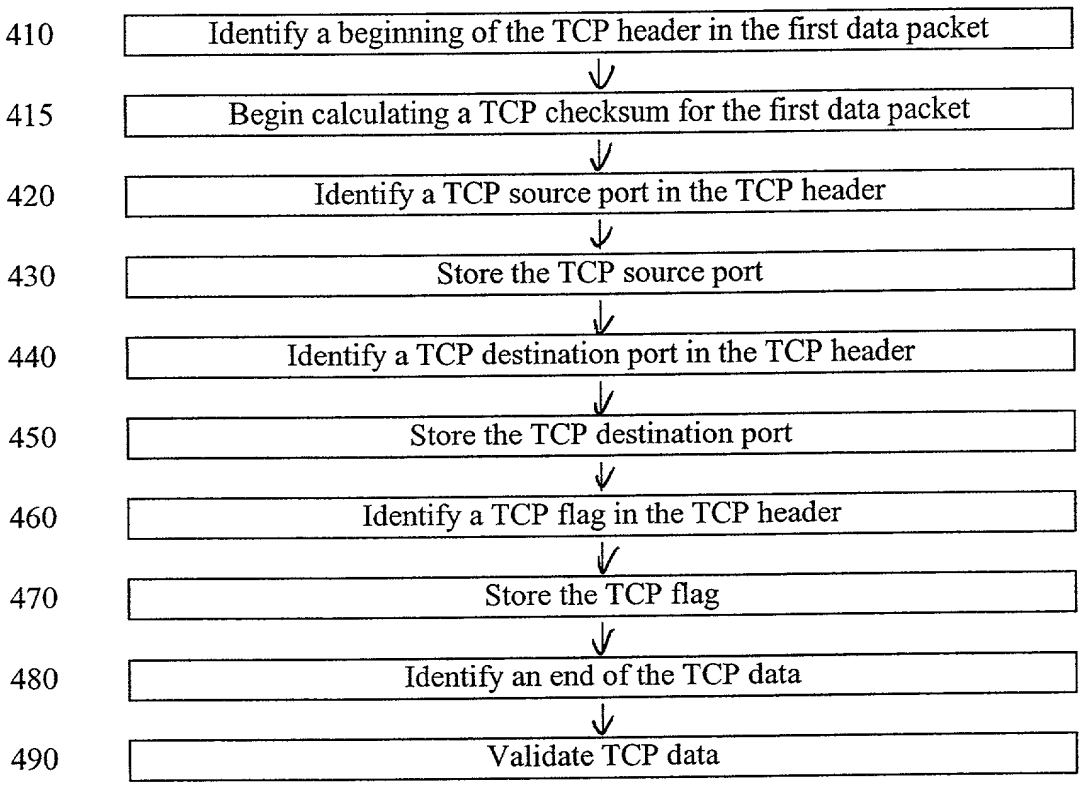

410
Identify a beginning of the TCP header in the first data packet
415
Begin calculating a TCP checksum for the first data packet
420
Identify a TCP source port in the TCP header
430
Store the TCP source port
440
Identify a TCP destination port in the TCP header
450
Store the TCP destination port
460
Identify a TCP flag in the TCP header
470
Store the TCP flag
480
Identify an end of the TCP data
490
Validate TCP data

FIG. 5

240

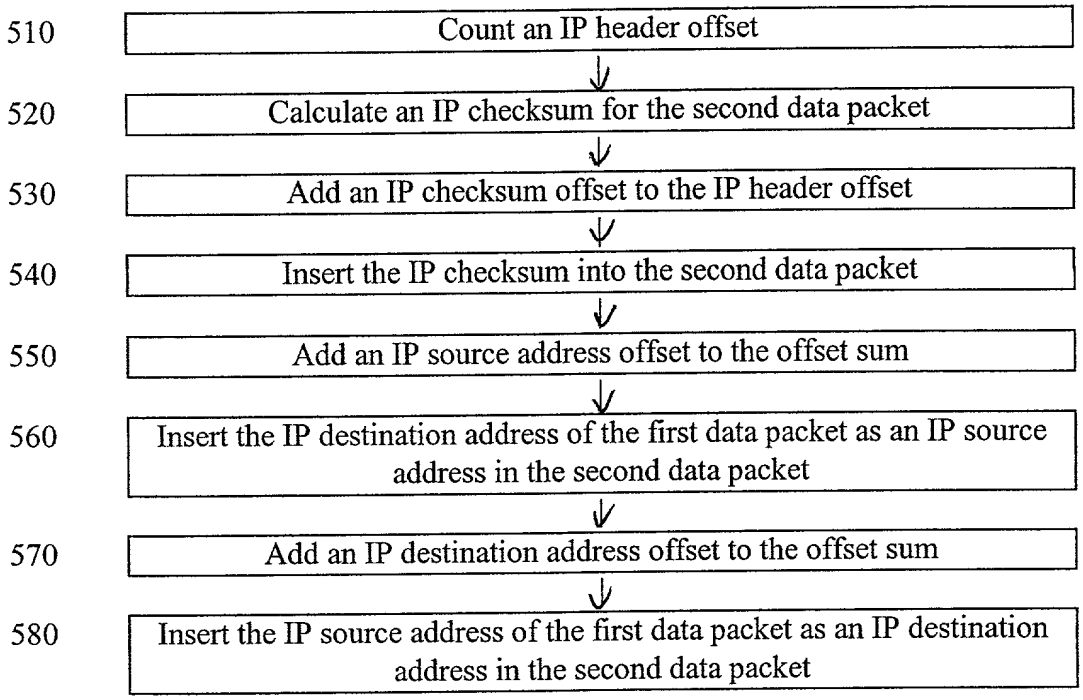
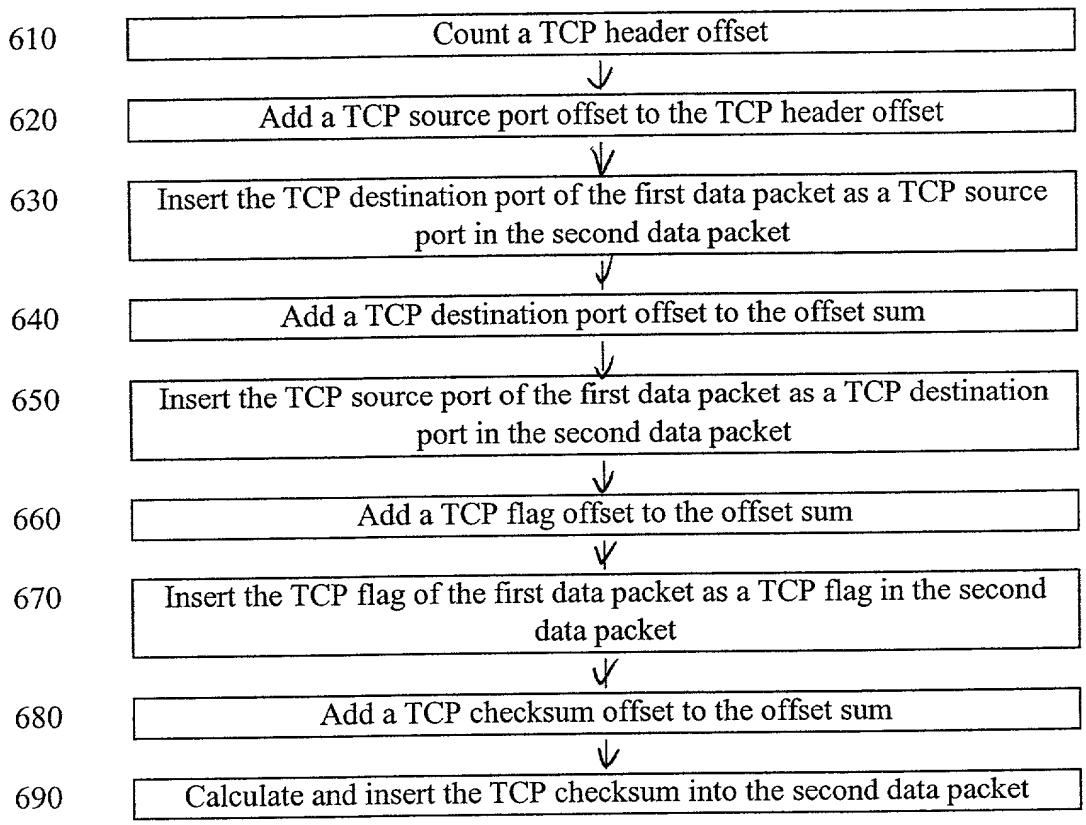

510
Count an IP header offset
520
Calculate an IP checksum for the second data packet
530
Add an IP checksum offset to the IP header offset
540
Insert the IP checksum into the second data packet
550
Add an IP source address offset to the offset sum
560
Insert the IP destination address of the first data packet as an IP source address in the second data packet
570
Add an IP destination address offset to the offset sum
580
Insert the IP source address of the first data packet as an IP destination address in the second data packet

FIG. 6


245
610
Count a TCP header offset
620
Add a TCP source port offset to the TCP header offset
630
Insert the TCP destination port of the first data packet as a TCP source port in the second data packet
640
Add a TCP destination port offset to the offset sum
650
Insert the TCP source port of the first data packet as a TCP destination port in the second data packet
660
Add a TCP flag offset to the offset sum
670
Insert the TCP flag of the first data packet as a TCP flag in the second data packet
680
Add a TCP checksum offset to the offset sum
690
Calculate and insert the TCP checksum into the second data packet

Attorney Docket No.: 115148

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ERROL GINSBERG
VALERIU COZLOVSCHI
JOEL WEISSBERGER
MARK McWHIRTER

Filed: Herewith

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

DECLARATION

As a below named inventor, I hereby declare that:

Type of Declaration

This declaration is made in an original application for utility patent.

Inventorship and Specification Identification

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled Method of Determining Time Delay for Round-Trip Transmission of Data and Electronic Apparatus Therefor, filed herewith.

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Inventors: GINSBERG; COZLOVSCHI; WEISSBERGER; and McWHIRTER

Declaration

Acknowledgment of Review of Papers and Duty of Candor

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims thereof.

I acknowledge the duty to disclose information that is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a).

Declaration

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signatures

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MONTROSE, CA 91020

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

Inventors: GINSBERG; COZLOVSCHI; WEISSBERGER; and McWHIRTER

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Attorney Docket No.: 115148

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

JOEL WEISSBERGER
MARK McWHIRTER
VALERIU COZLOVSCHI
ERROL GINSBERG

Filed: Herewith

Title: METHOD OF DETERMINING TIME DELAY FOR ROUND-TRIP TRANSMISSION OF DATA AND ELECTRONIC APPARATUS THEREFOR

POWER OF ATTORNEY

IXIA Communications is the owner of the above-identified patent, pursuant to an Assignment from the owners of record, Joel Weissberger, Mark McWhirter, Valeriu Cozlovschi, and Errol Ginsberg to IXIA Communications executed on 6/2/00 (the "Assignment"). In accordance with 37 C.F.R. § 3.73(b), a copy of the Assignment is attached hereto. A copy of the Assignment has also been filed or is being filed contemporaneously herewith for recordation with the Assignment Branch.

IXIA Communications hereby revokes all previous powers of attorney and appoints John T. Jones, Reg. No. 45,550; Susan Stone Rosenfield, Reg. No. 36,287, and George C. Chen, Reg. No. 39,935 of the firm of Bryan Cave LLP, Two North Central Avenue, Suite 2200, Phoenix, Arizona, 85004, telephone (602) 364-7000, facsimile (602) 364-7000, as its attorneys with full powers of substitution, revocation and association, to transact all business in the United States Patent and Trademark Office in connection with the above-identified patent application.

Please direct all correspondence regarding this patent application to George C. Chen, Bryan Cave LLP, Two North Central Avenue, Suite 2200, Phoenix, Arizona 85004, phone (602) 364-7000.

IXIA COMMUNICATIONS

Dated: 6/2/00

By: E Ginsberg

Name: Errol Ginsberg

Title: President

256965